



H55H-M3 V :1.0

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REVISION HISTORY:

Rev	Date	Notes
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IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.



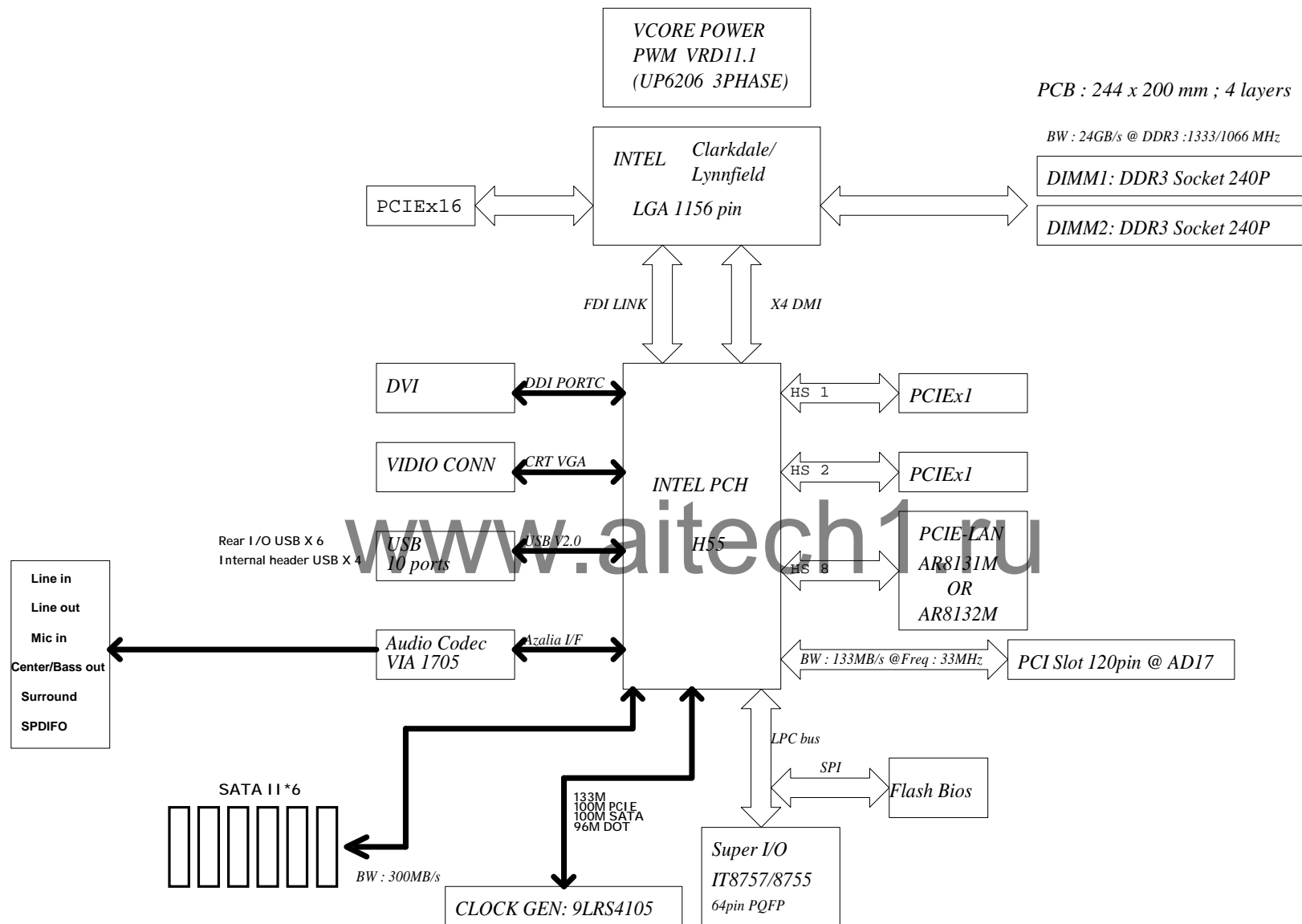
2) DESIGN NOTES in yellow are notes of caution.




3) DESIGN NOTES in red are critical, and must be understood and followed.

PCB STACK: L1:TOP
L2:VCC
L3:GND
L4:BOTTOM

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Title Cover Page		
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 Elitegroup Computer Systems			
Block Diagram			
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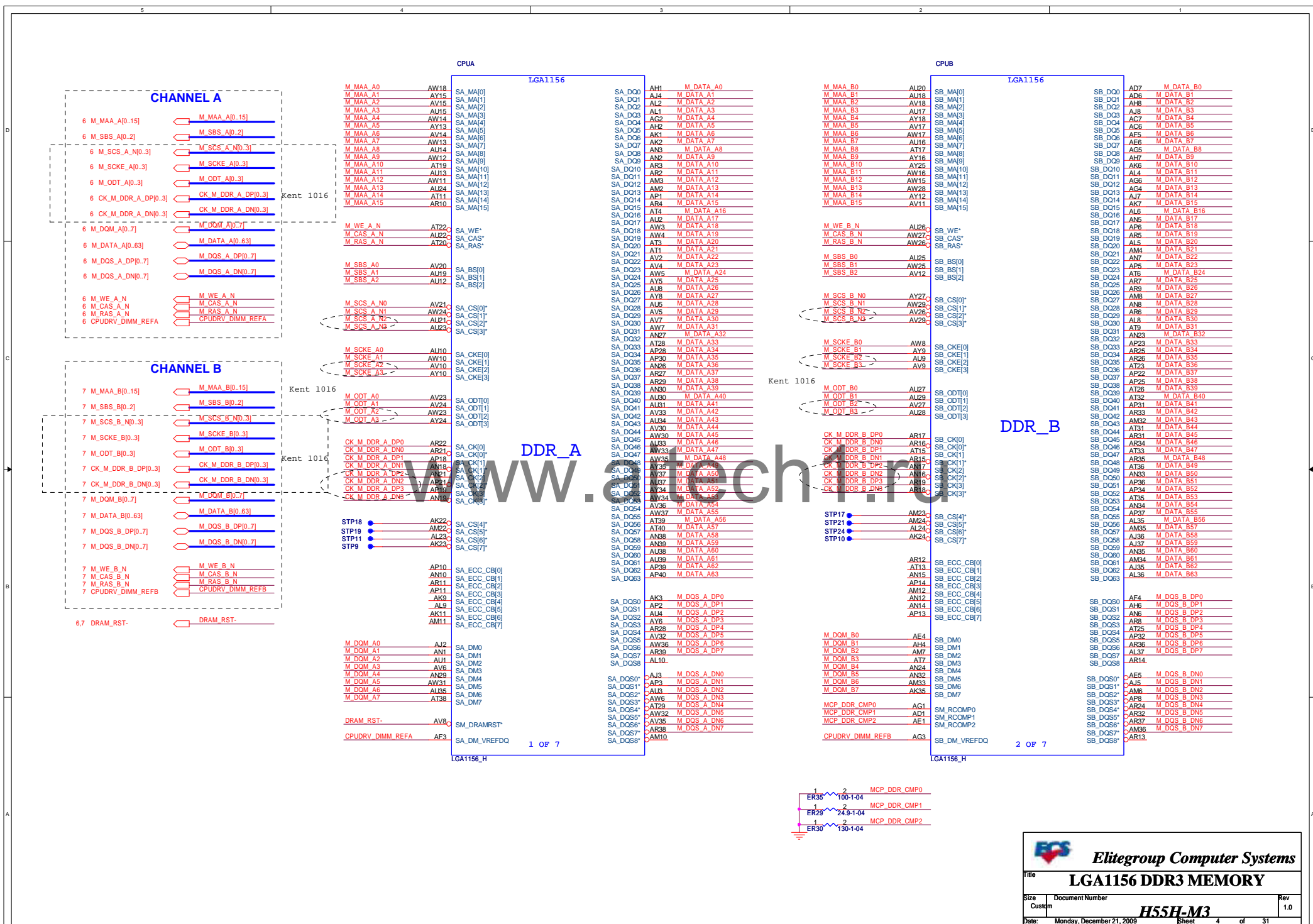
POWER ON CONFIG (POC) TABLE		
VID0	FUNCTION	DEFAULT
VID0	MS10	
VID1	MS11	011:Supprot CKD6 Id
VID2	MS12	
VID3	IMON_CONFIG0	
VID4	IMON_CONFIG1	101: Icc(MAX) =120A
VID5	IMON_CONFIG3	
VID6	RESERVED	
VID7	VRD_SELECT	LOW
PSI#	RESERVED	LOW

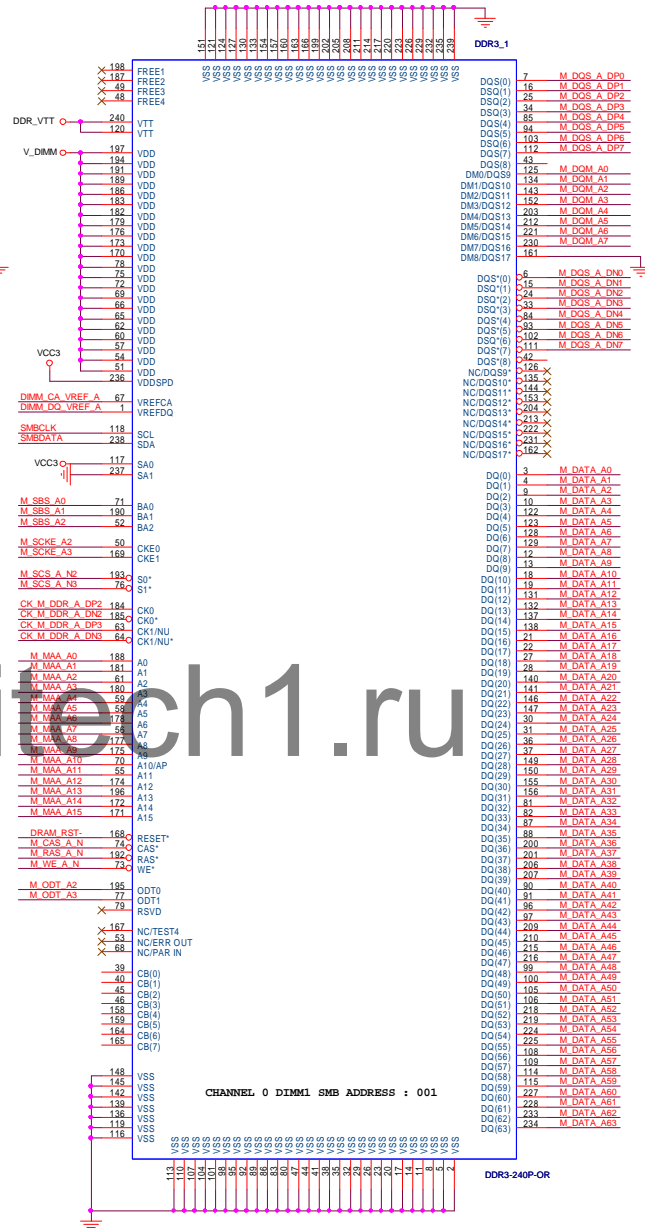
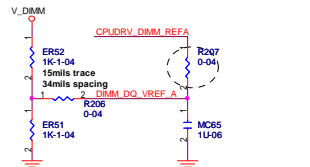
CFG	H	L	DESCRIPTION
0	RSVD		PEG SEL0
1	RSVD		PEG SEL1
2	RSVD		PEG SEL3
3	NRM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENT
5	RSVD		
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		ENGINEERING EXPERIMENT
			15: HWY INTERNAL

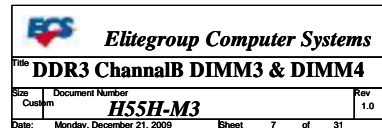
PEG CONFIG TABLE

SEL2	SEL1		PCIE CONFIG
1	1 1	SEL0	1 X 16
1	1	0	2 X 8

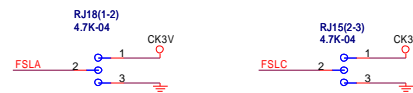
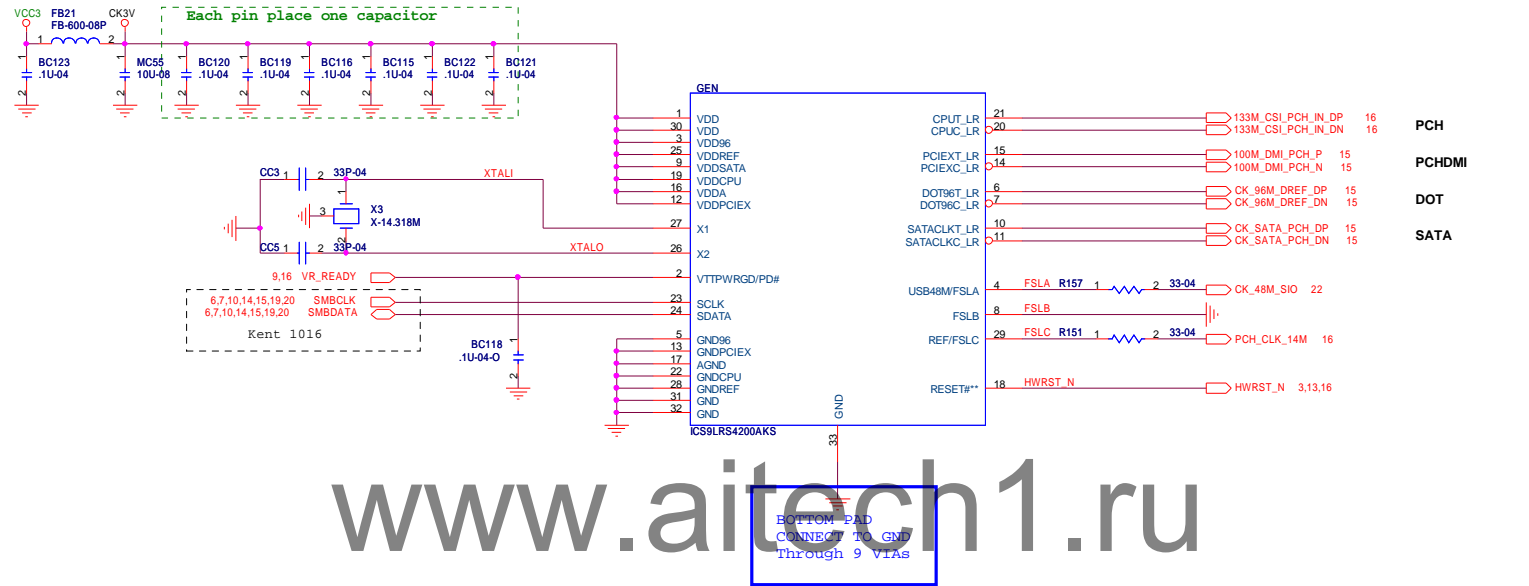
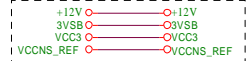






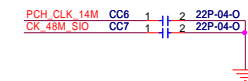


External Connection



FSLC,FSLB,FSLA = 001, CPU_CLK = 133MHz

FSLC (B0b2)	FSLB (B0b1)	FSLA (B0b0)	CPU MHz	PCIEX MHz	SATA MHz	DOT96 MHz
0	0	1	133.33	100	100	96.00
1	0	1	100.00	100	100	96.00



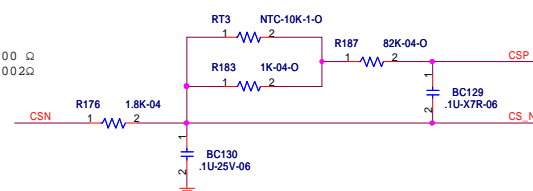
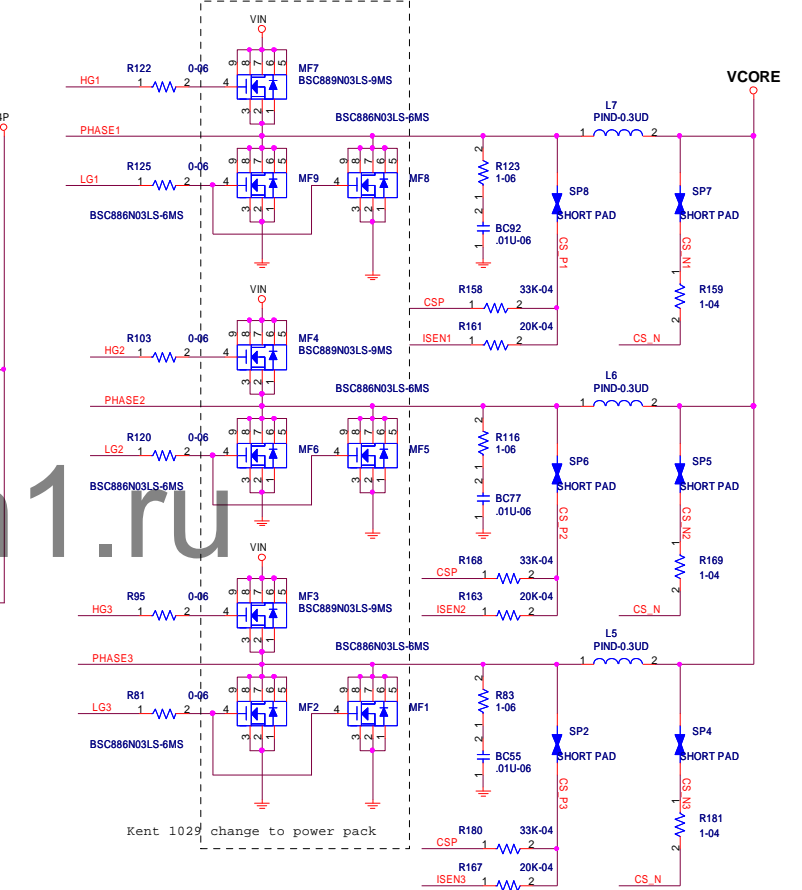
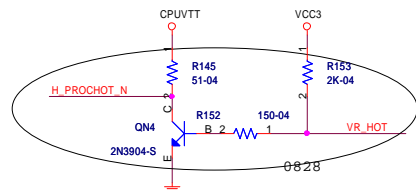
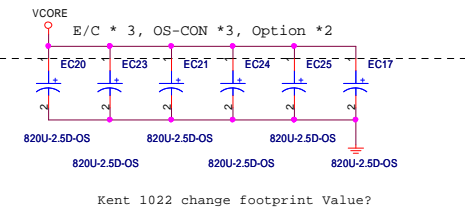
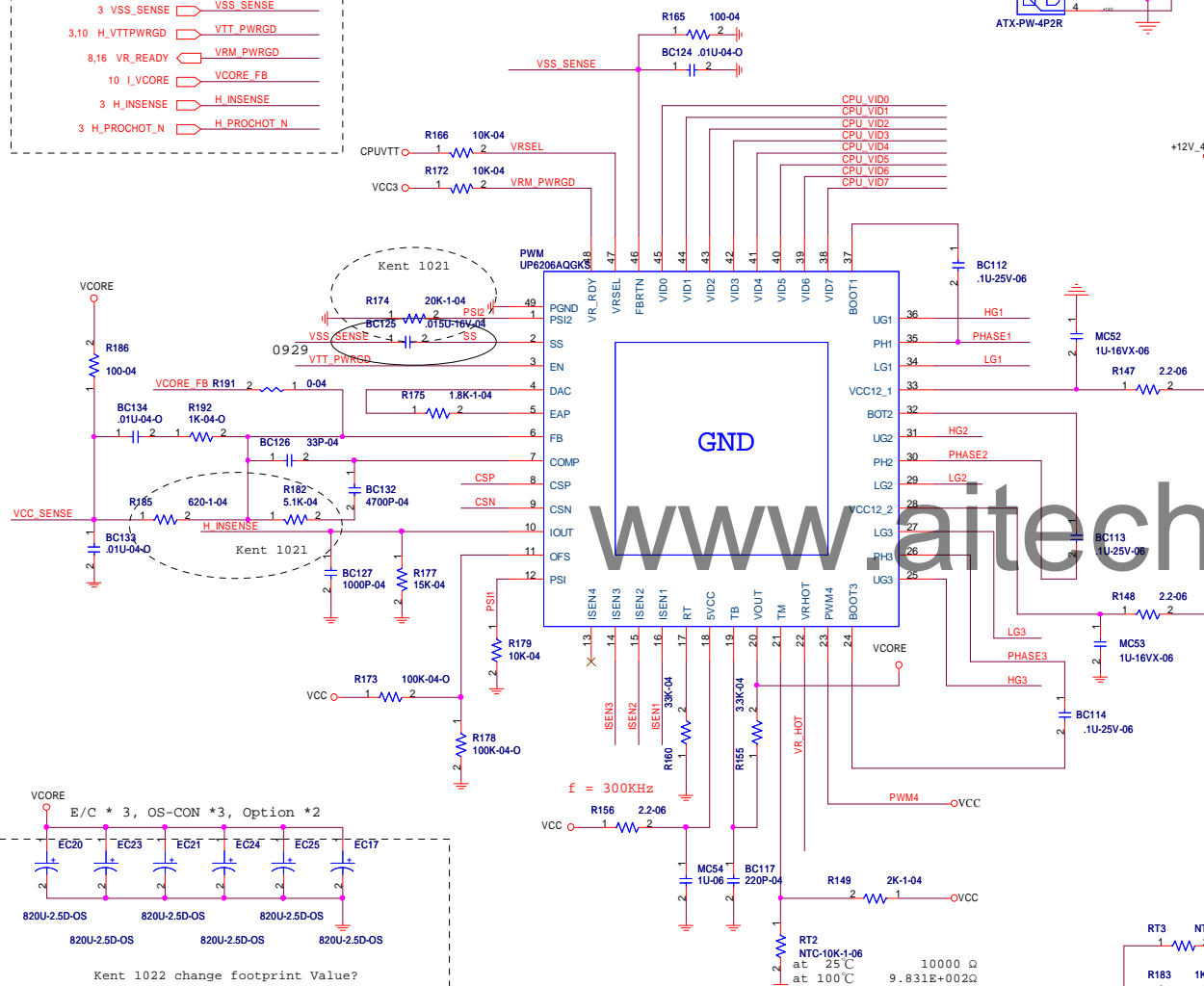
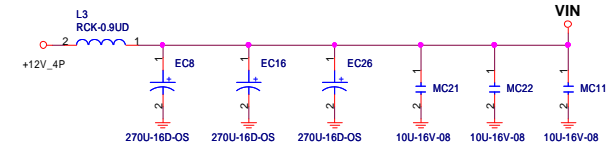
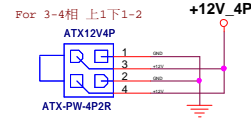
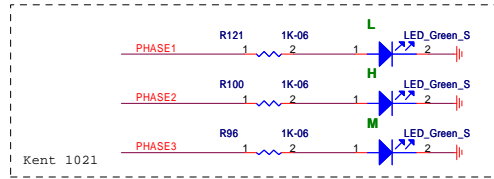
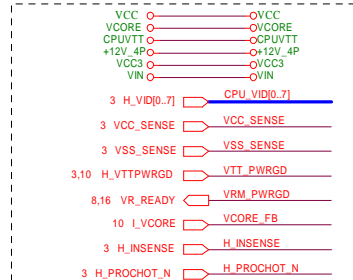
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File: **CLK 9LRS4200**

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External Connection

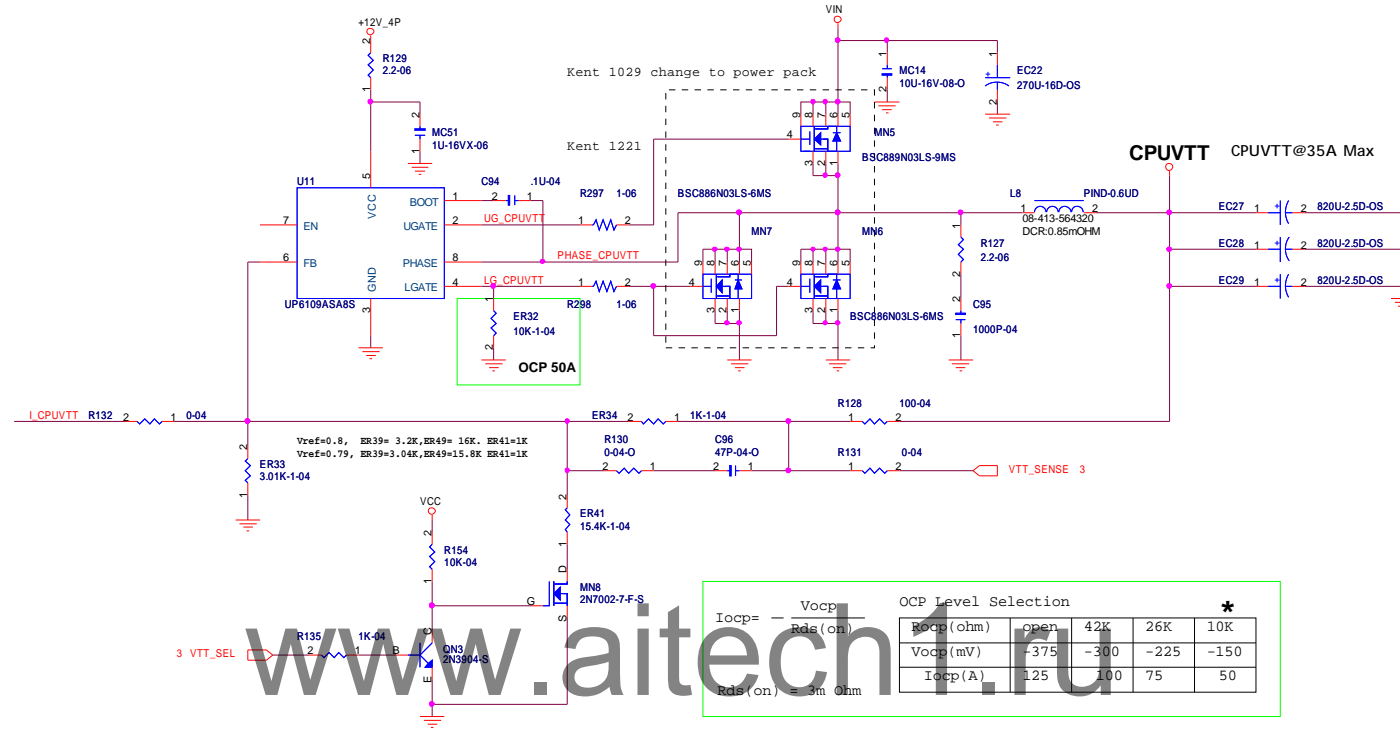


Elitegroup Computer Systems			
Title			
CPU VCORE UP6206			
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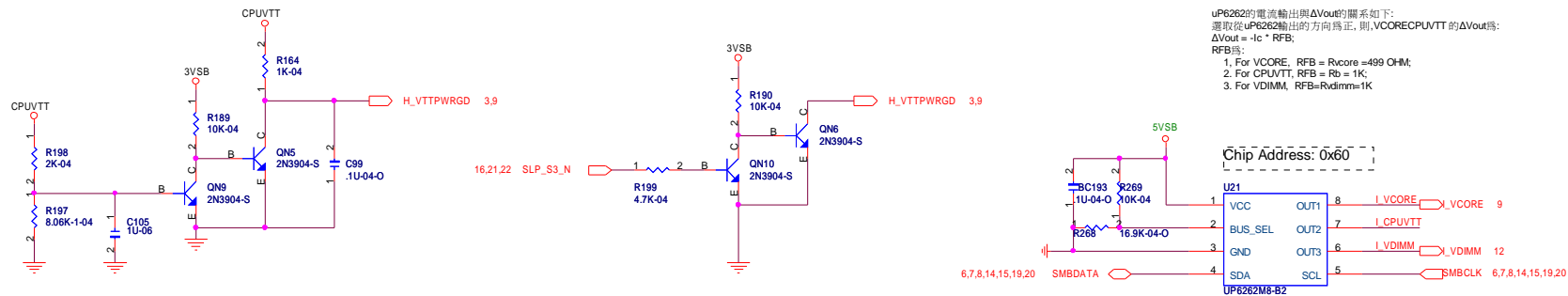
+12V_4P	○	+12V_4P
VIN	○	VIN
VCC	○	VCC
CPUVTT	○	CPUVTT
3VSB	○	3VSB
5VSB	○	5VSB

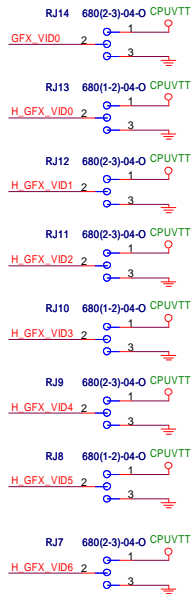
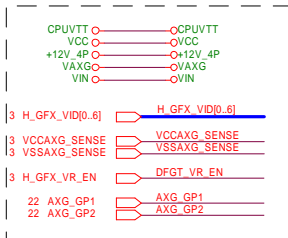
VTT_SEL	CPUVTT
1	1.05V
0	1.10V



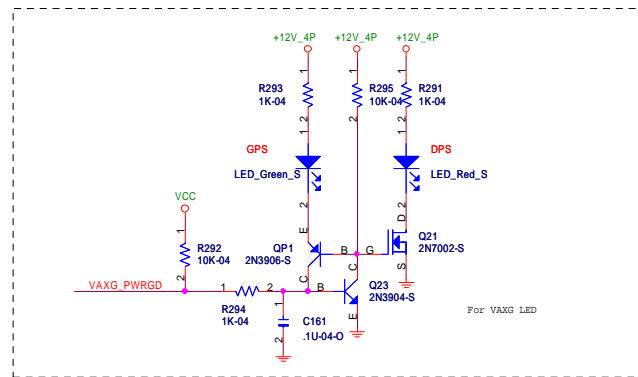
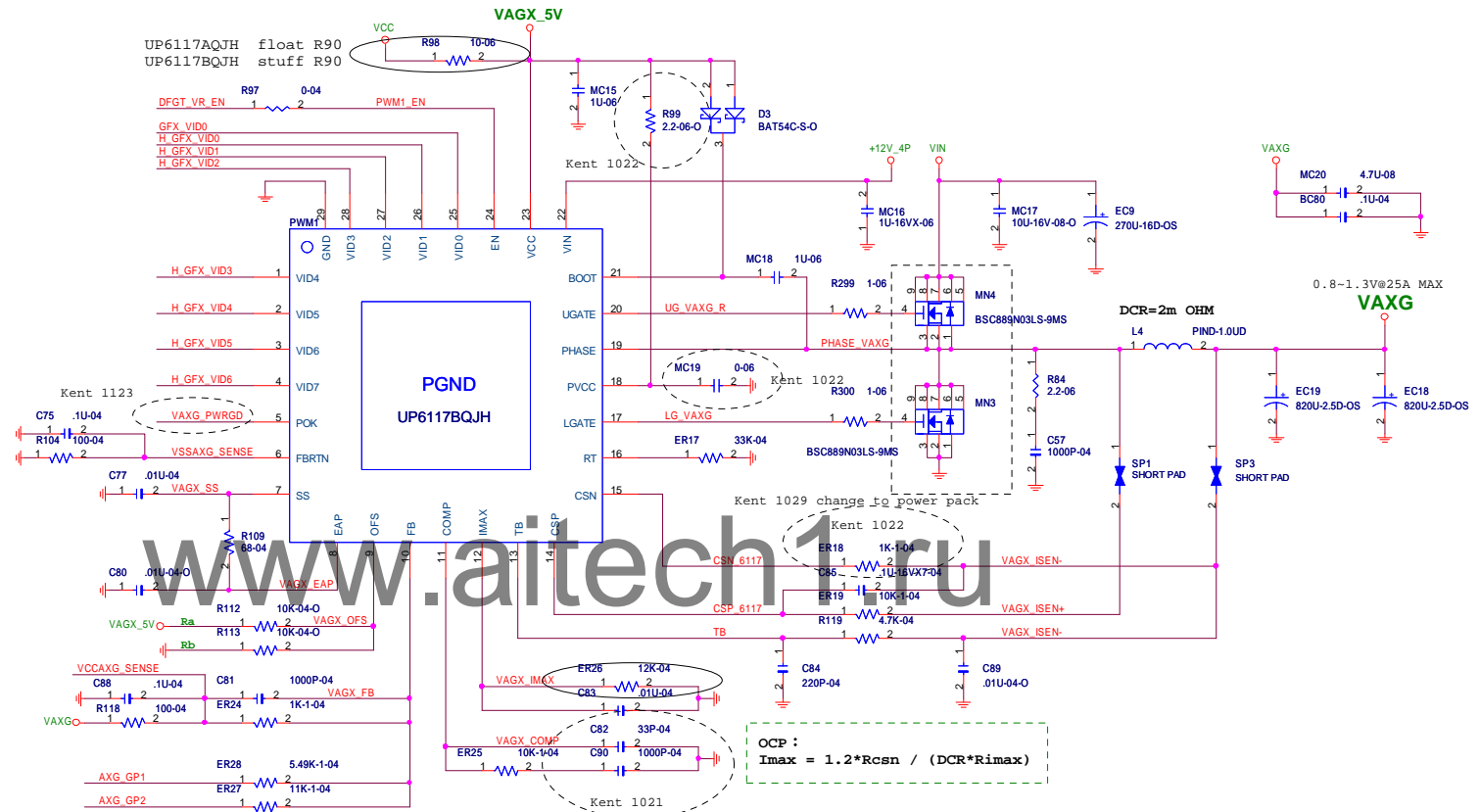
$I_{ocp} = \frac{V_{ocp}}{R_{ds(on)}}$		OCP Level Selection *			
Rocp (ohm)	open	42K	26K	10K	
Vocp (mV)	-375	-300	-225	-150	
Iocp (A)	125	100	75	50	


$R_{ds(on)} = 3m\ \Omega$



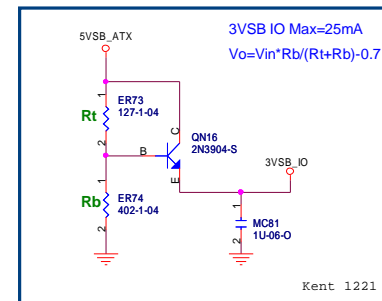
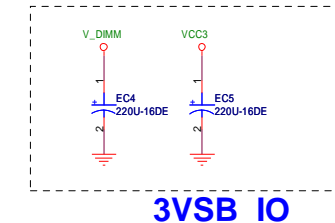
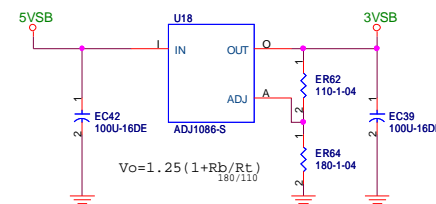
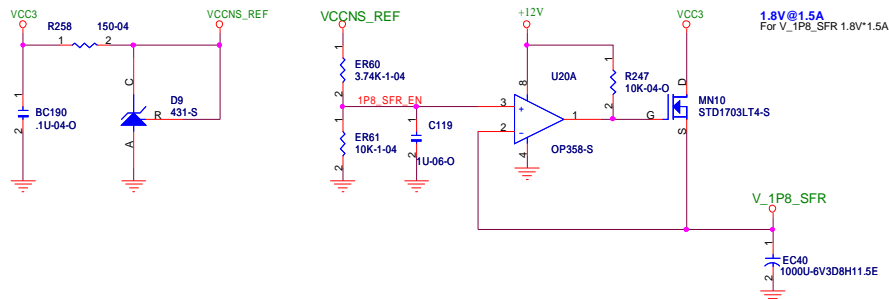
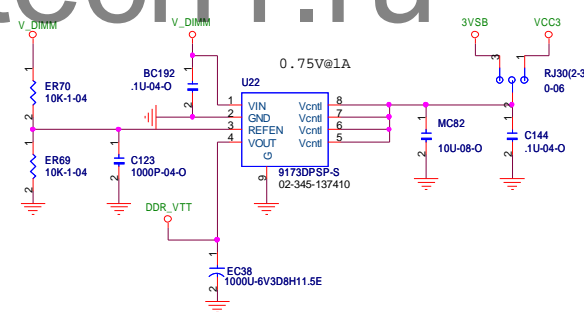
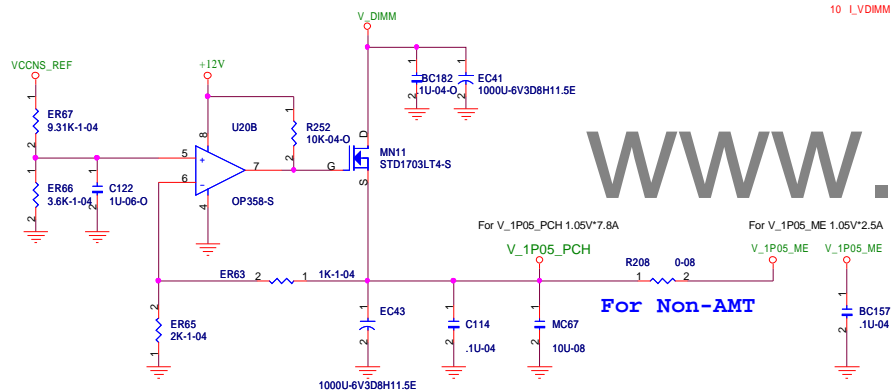
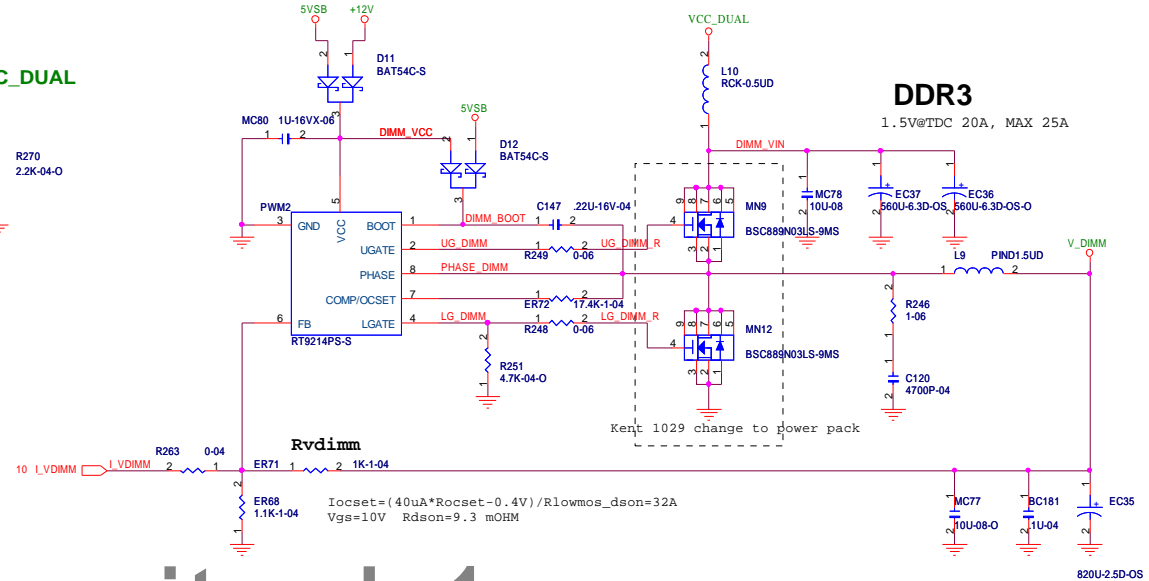
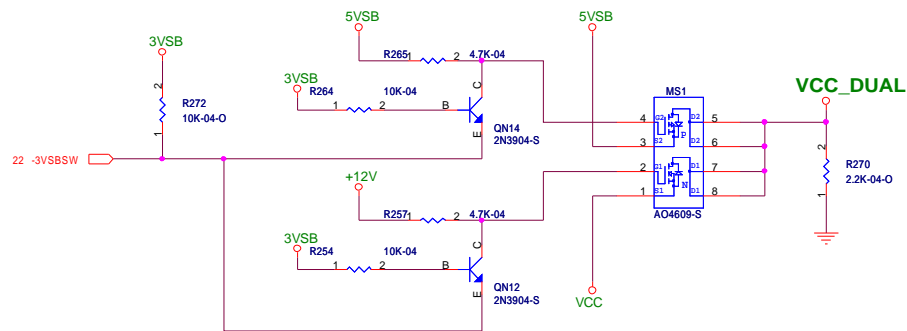


AXG_GP1	AXG_GP2	Vaxg
1	1	+0 mV
1	0	+100mV
0	1	+200mV
0	0	+300mV



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CPU VAXG POWER UP6117A			
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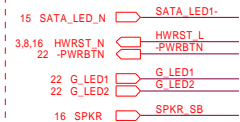
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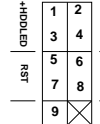
Elitegroup Computer Systems			
DC-DC DUAL VDIMM			
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FRONT PANEL

External Connection



F_PANEL

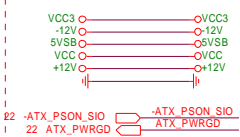


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	B	L	L	L
	G	GB	YB	OFF	OFF

B: Blinking

POWER CONNECTOR

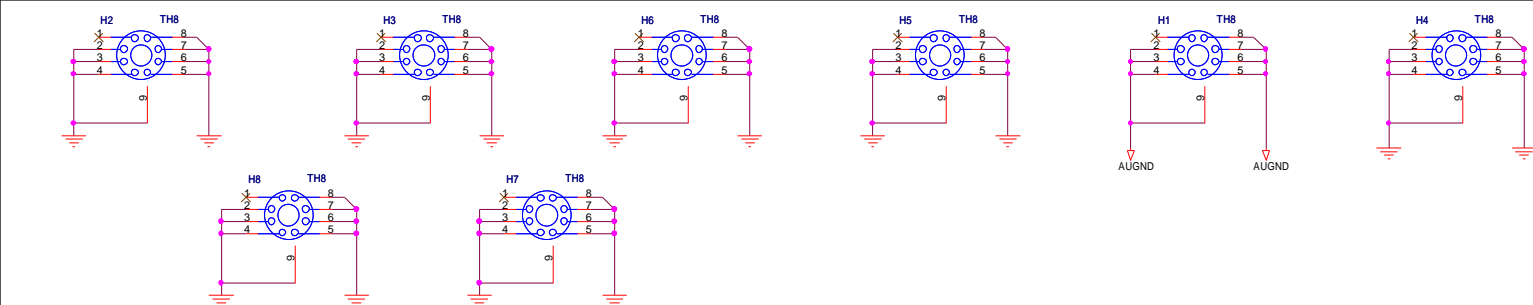
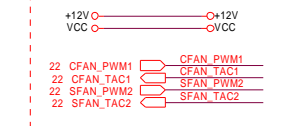
External Connection



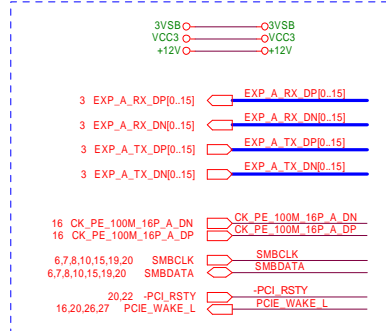
FAN

Kent 1016

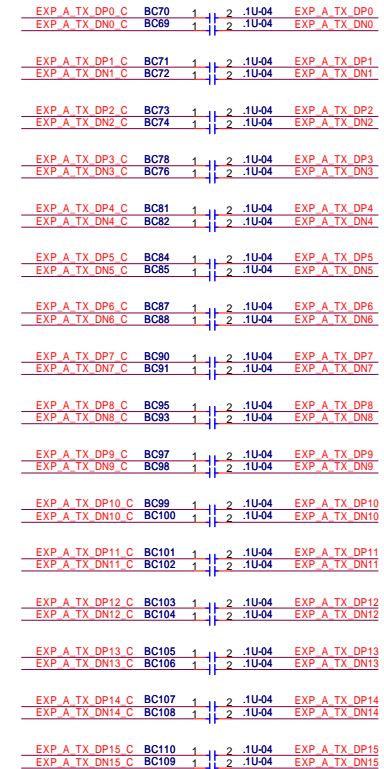
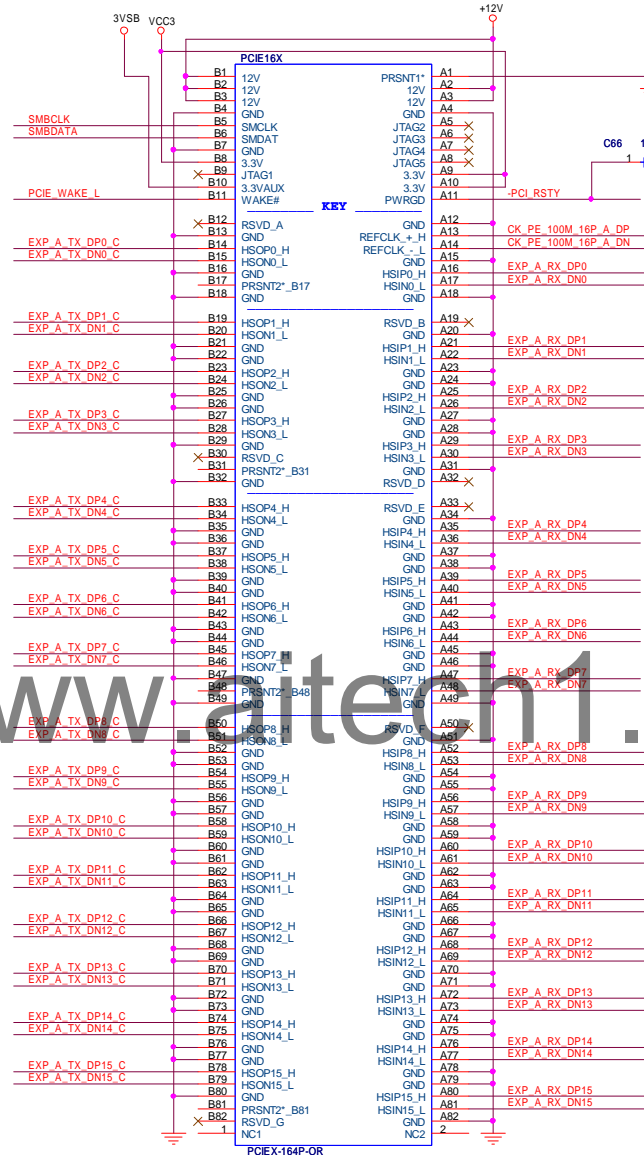
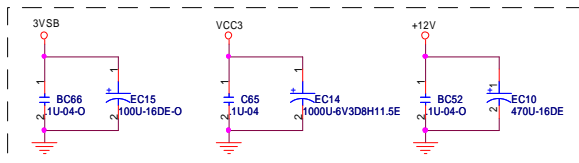
External Connection



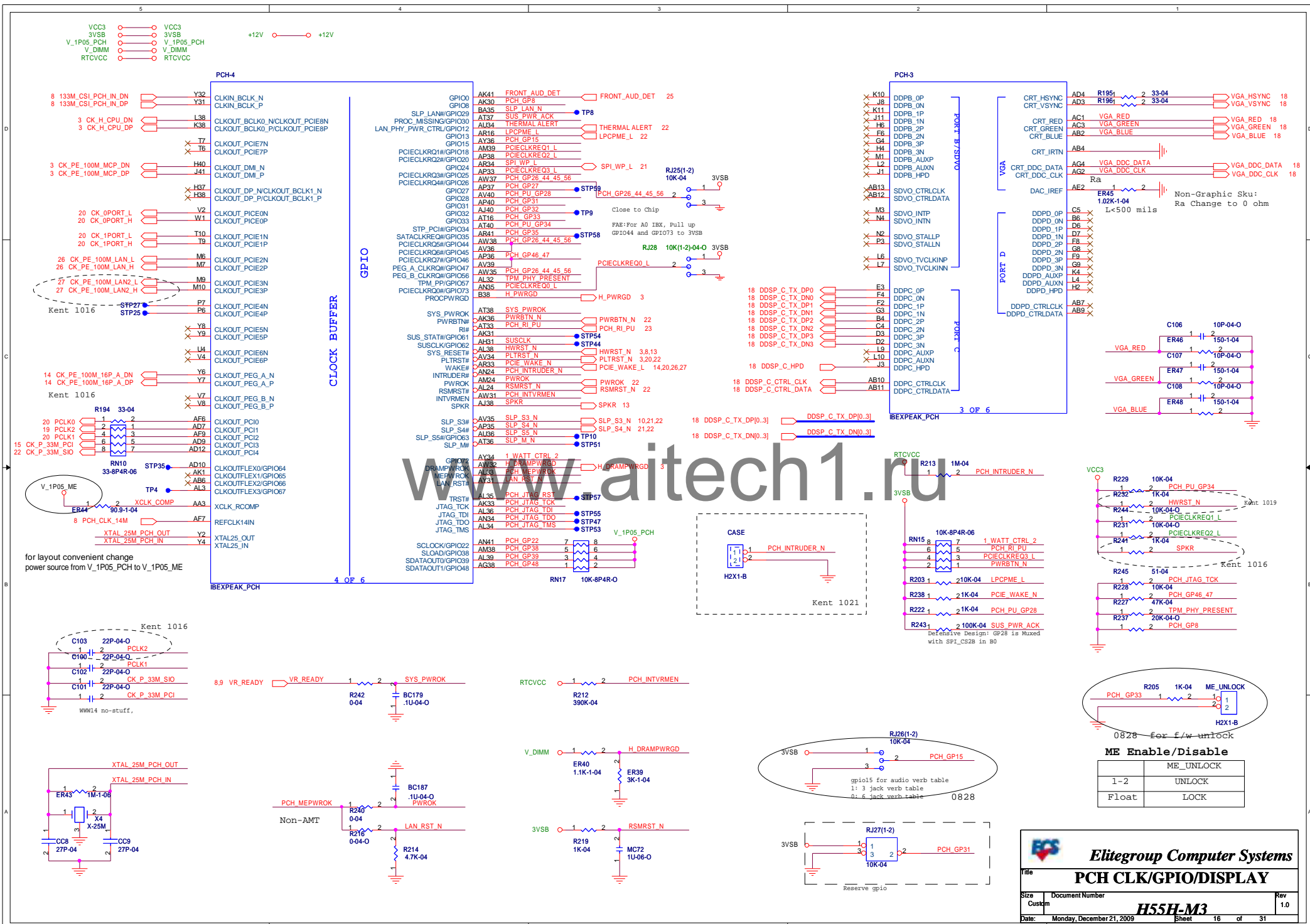
PCIEX16 External Connection



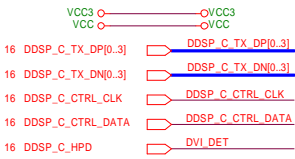
Please place the caps close to PCI-EX16 Slot.



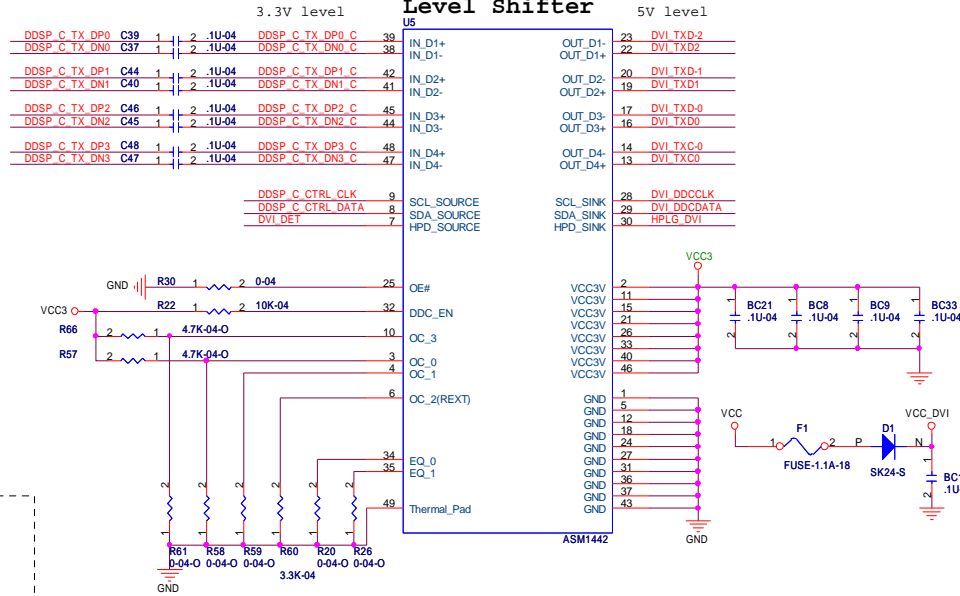




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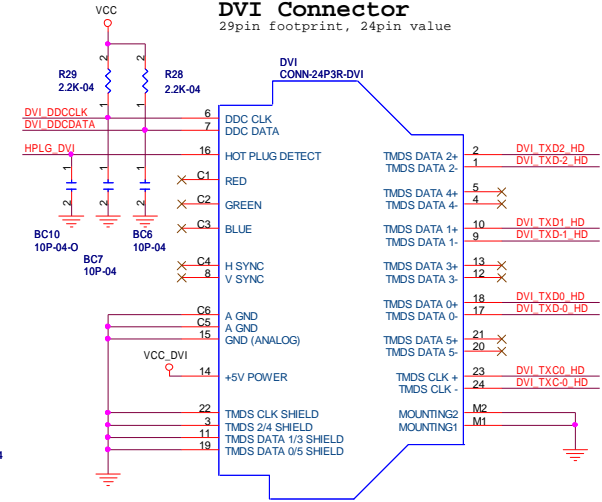


Level Shifter



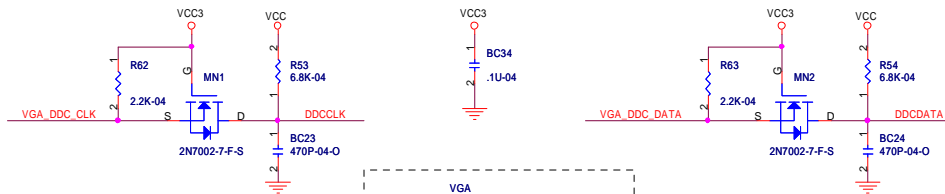
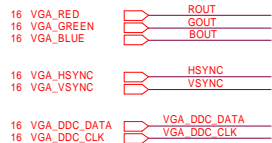
DVI Connector

29pin footprint, 24pin value

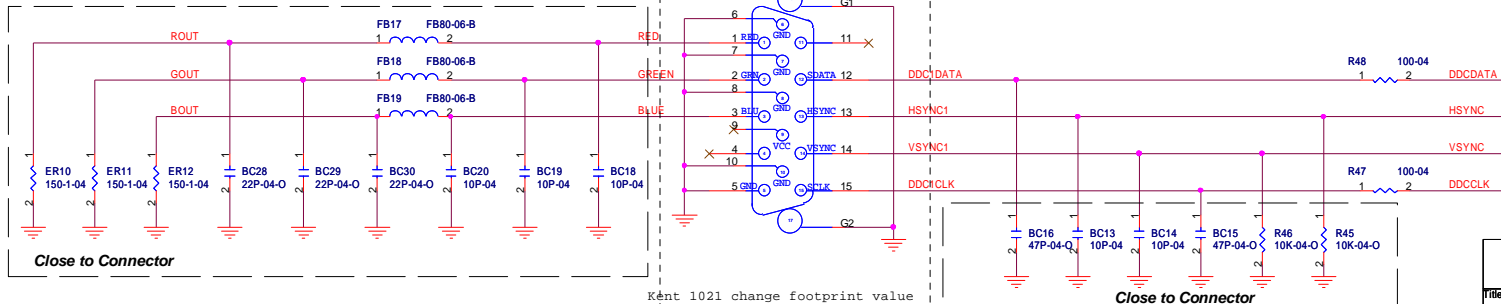
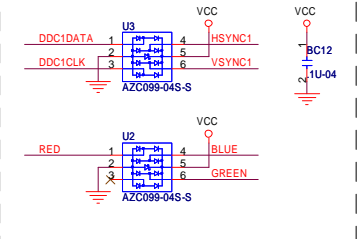


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External Connection

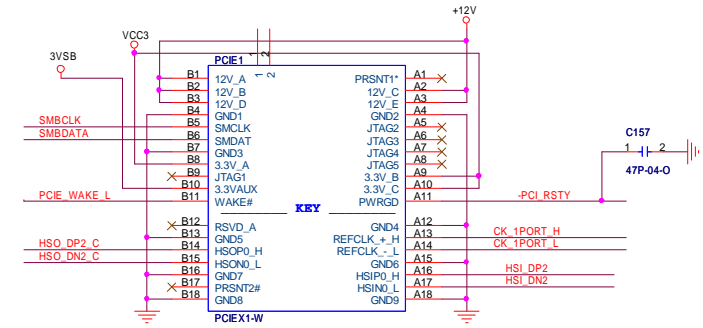
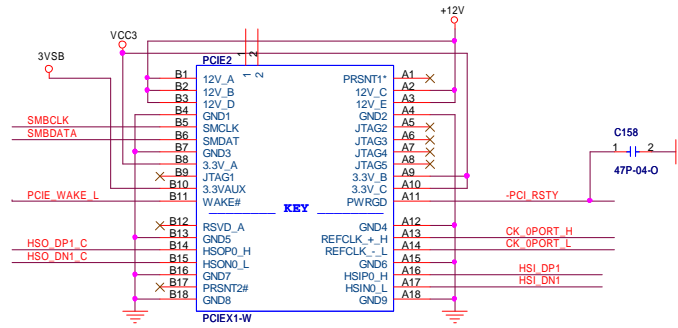
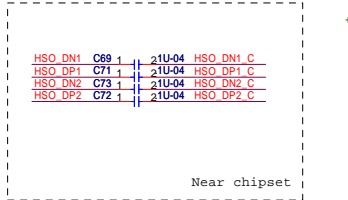
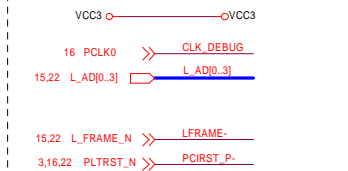
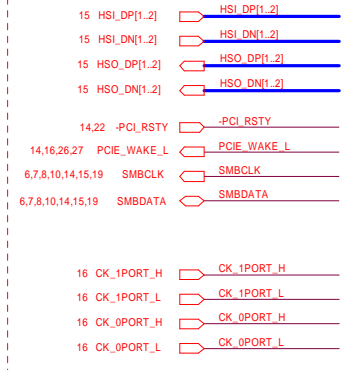


ESD

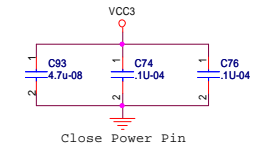
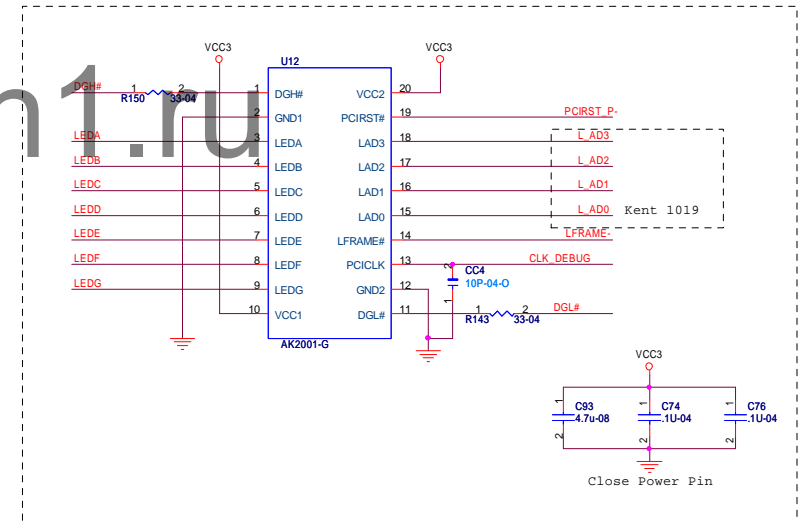


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DVI, RGB			
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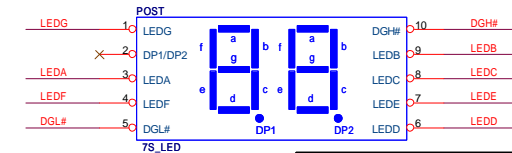
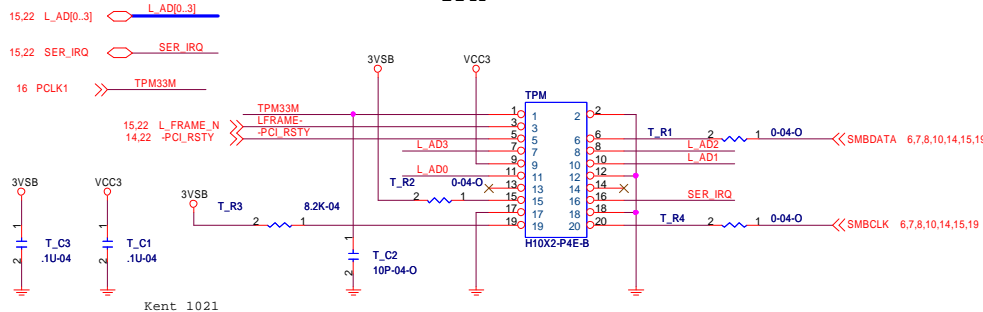
External Connection



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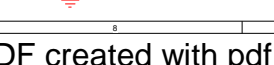
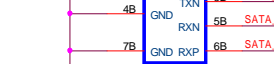
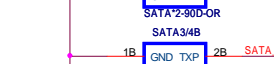
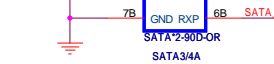
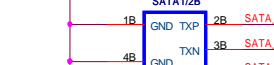
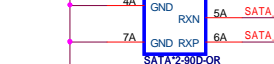
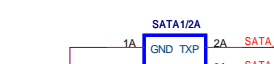
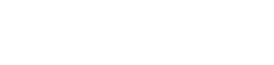
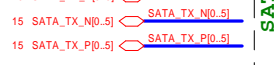
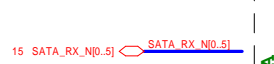
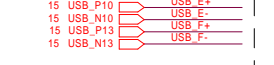
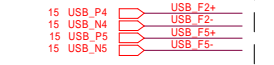
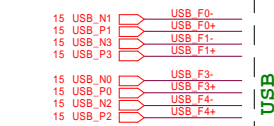


TPM



Elitegroup Computer Systems		
PCIEX4/X1		
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External Connection



FRONT_SIDE

FRONT_SIDE

FRONT_SIDE

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FRONT_SIDE

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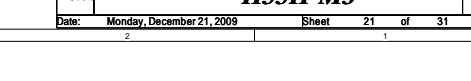
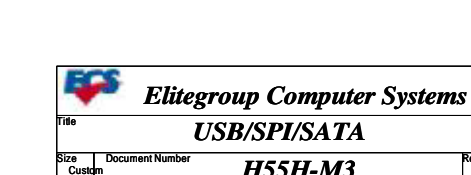
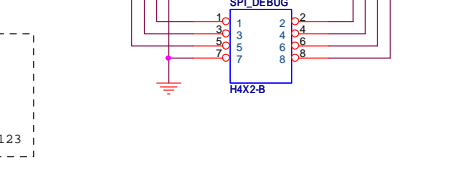
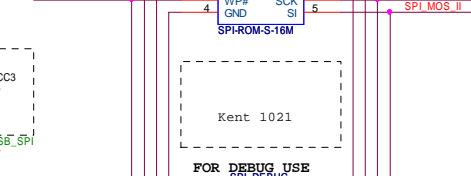
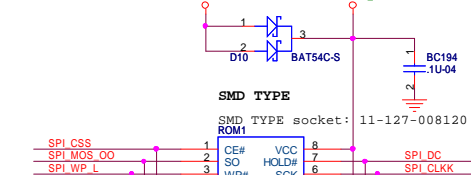
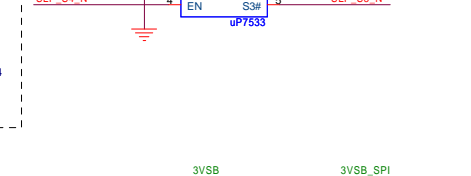
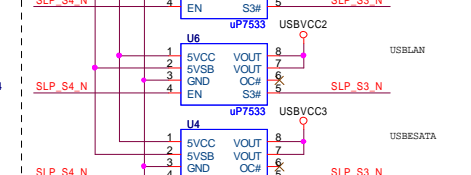
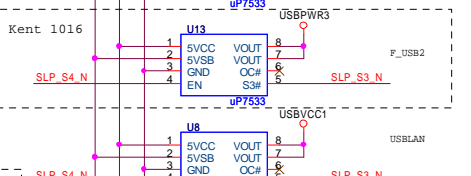
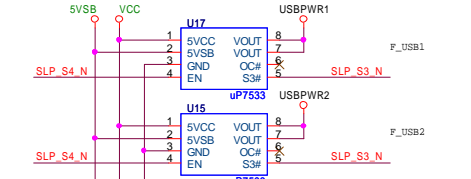
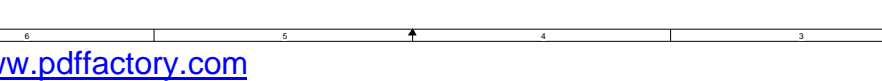
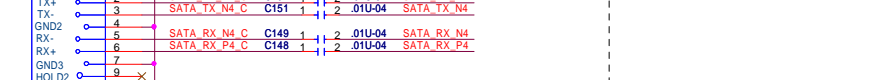
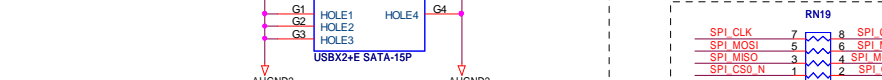
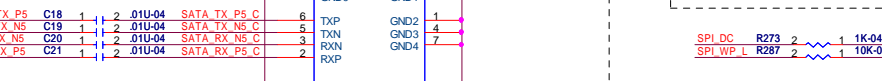
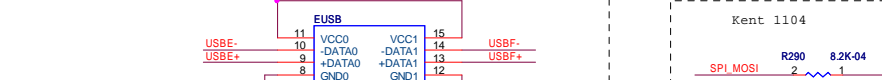
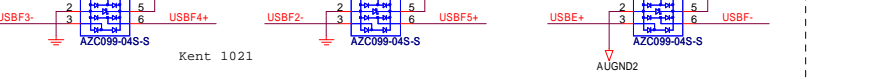
FRONT_SIDE

FRONT_SIDE

FRONT_SIDE

FRONT_SIDE

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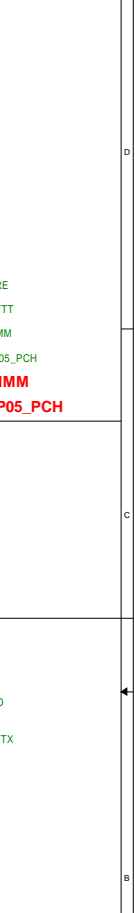
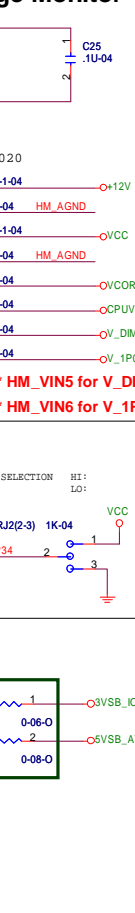
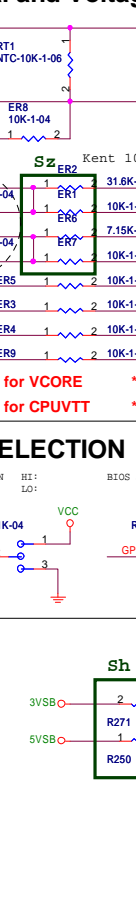
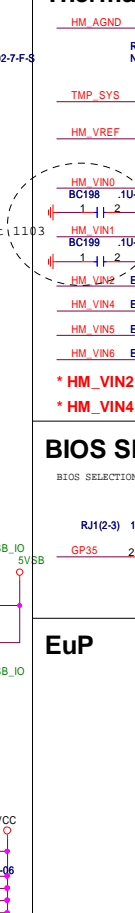
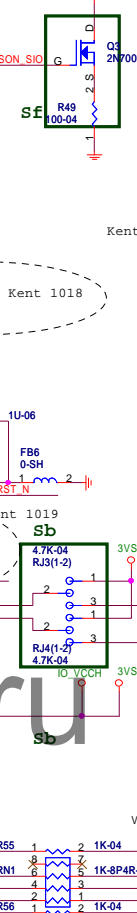
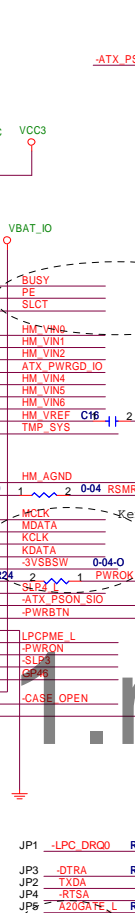
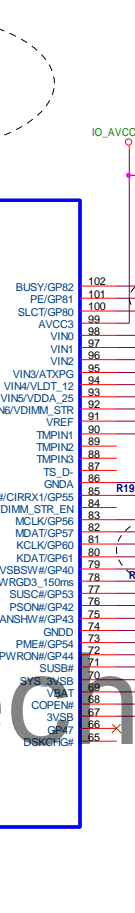
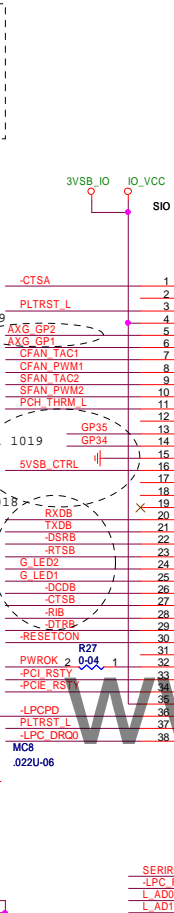
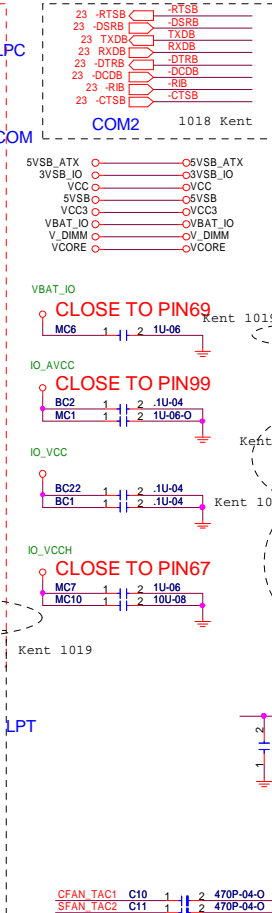
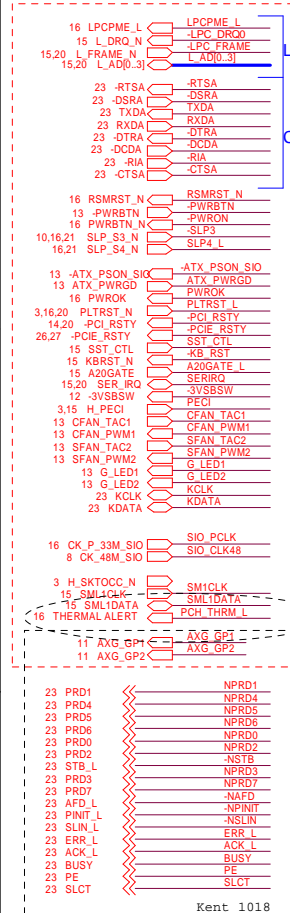
Elitegroup Computer Systems

USB/SPI/SATA

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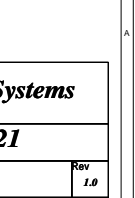
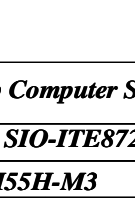
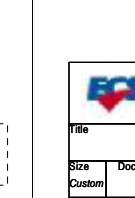
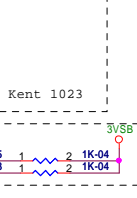
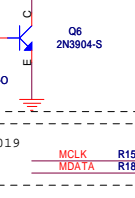
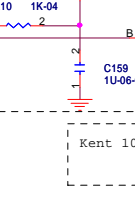
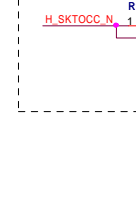
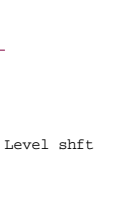
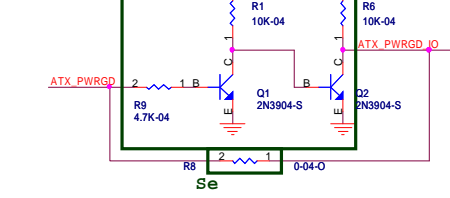
External Connection



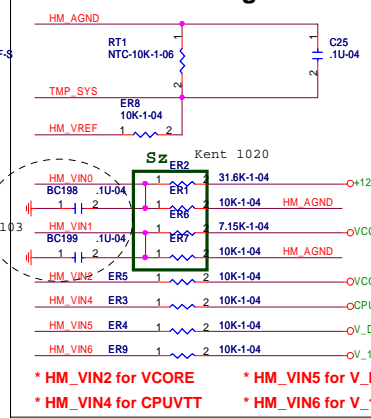
*IT8721 BX
Sa IT8721 BX
Sb (1-2)
Sc (1-2)
Sd 0-04
Se X
Sf V
Sh X
Sq V
Sz V

HW STRAPPING

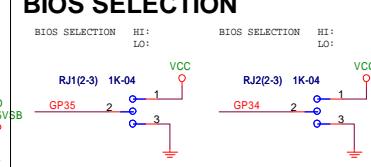
JP1 Pin 38	Flashsegt1_EN	Disabled
JP2 Pin 122	VIDO_EN	Disable VID output pins
JP3 Pin 124	CHIF_SEL	Chip selection in Configuration
JP4 Pin 128	KBPWR_EN	KB power sequence function is disabled
JP5 Pin 124	FAN_CTL_SEL	The default value of EC index 15h/16h/17h is 00h
JP6 Pin 46		The default value of EC index 15h/16h/17h is 40h
JP7 Pin 124		The default value of EC index 15h/16h/17h is 20h
JP8 Pin 124		The default value of EC index 15h/16h/17h is 7fh
JP9 Pin 46	WDT_EN	Disable WDT to rest PWROK
JP10 Pin 29	SVID_EN	Enable SVID Function



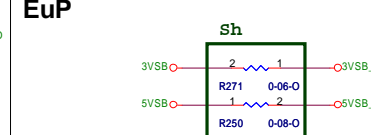
Thermal and Voltage Monitor



BIOS SELECTION



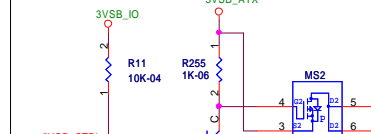
EuP



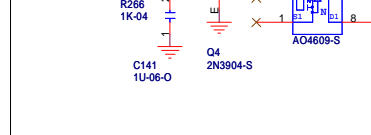
Sh



Sb



Sc



Sd



Se



Elitegroup Computer Systems

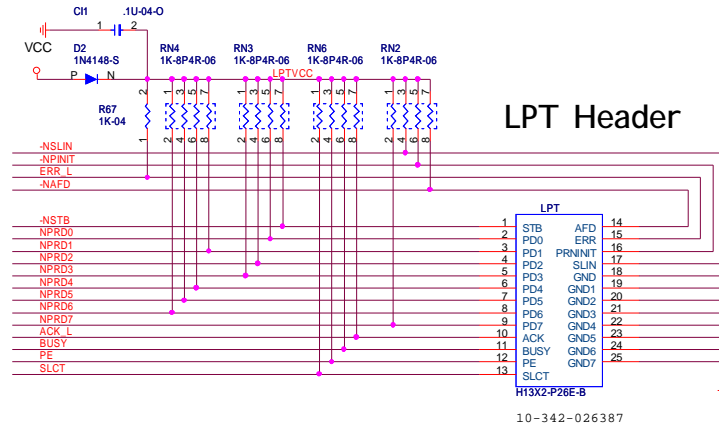
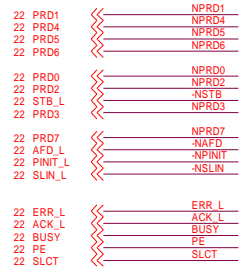
LPC SIO-ITE8721

H55H-M3

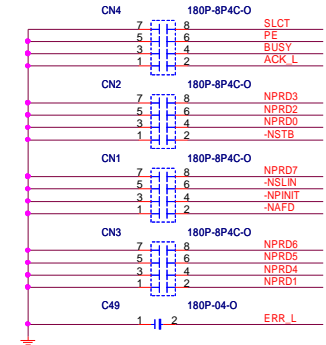
Size: Custom Document Number: Monday, December 21, 2009 Sheet 22 of 31

LPT Ports

External Connection



LPT Header

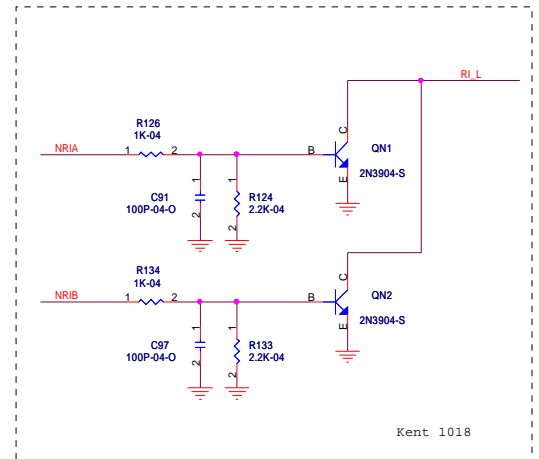
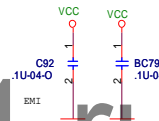
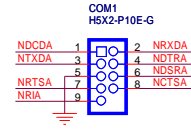
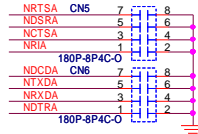
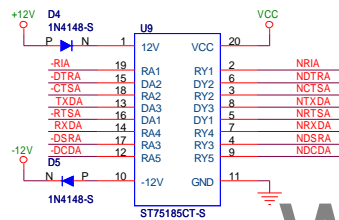
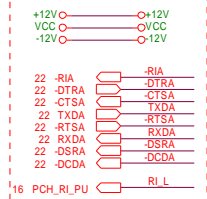


Kent 1018

10-342-026387

COM Ports

External Connection

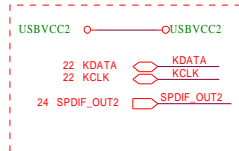


Kent 1018

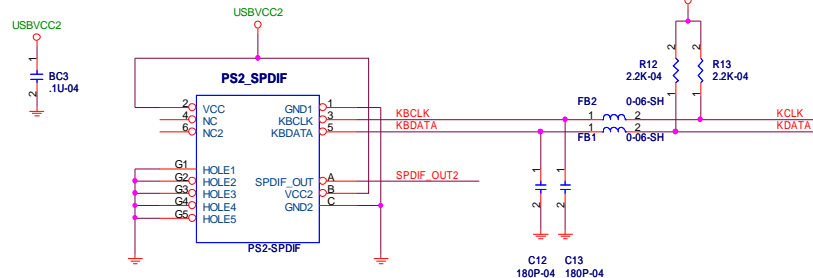
Kent 1018

PS_SPDIF

External Connection



PS_SPDIF I/O CONNECTOR



Elitegroup Computer Systems

LPT, COM, PS_SPDIF

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Monday, December 21, 2009

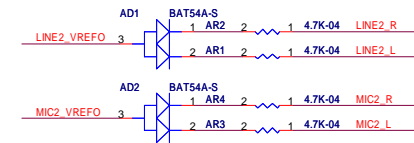
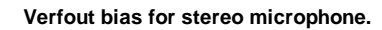
Sheet 23 of 31

16.25 FRONT_AUD_DET 16.25

For AC97 Header Judgement
GPI to South Bridge

Kent 1019

CODEC



NetA

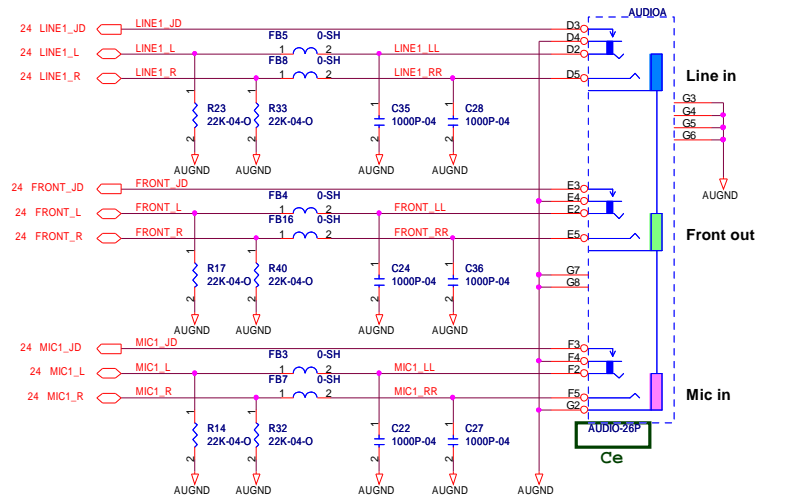
Input Node	Weight	Output Node	Output Value
AER7	5.1K-1.04	FRONT_JD	25
AER9	10K-1.04	LINE1_JD	25
AER8	20K-1.04	MIC1_JD	25
AER10	39.2K-1.04	SURR_JD	25

NetB

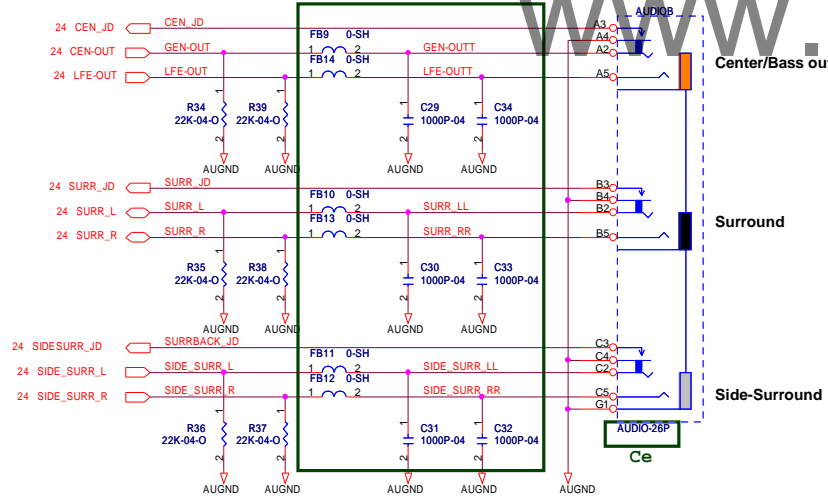
Input Node	Weight	Output Node	Output Value
AER4	10K-1.04	CEN_JD	25
AER1	20K-1.04	MIC2_JD	25
AER5	39.2K-1.04	LINE2_JD	25
AER3	5.1K-1.04	SIDESURR_JD	25
AER2	47-1.04-0	F_SENSE	25

 Elitegroup Computer Systems			
Title AUDIO ALC892 (CHIP)			
Size Custom	Document Number <div style="text-align: center; font-size: 1.2em;">H55H-M3</div>	Rev 1.0	
Date: Wednesday, December 23, 2009		Sheet 24	of 31

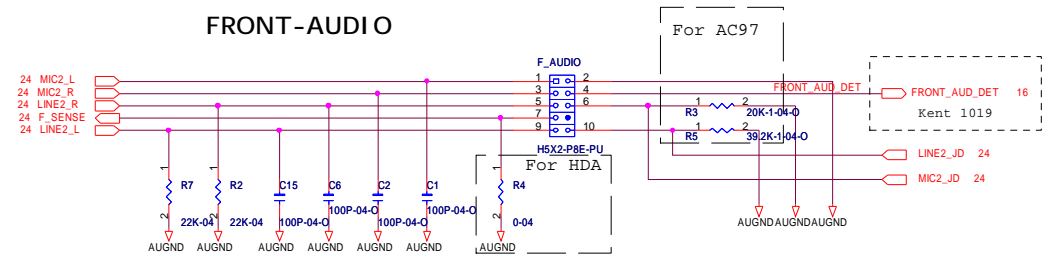
REAR-AUDIO



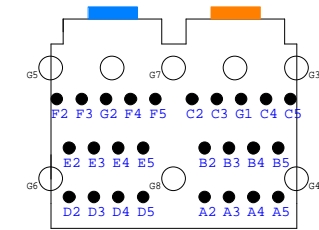
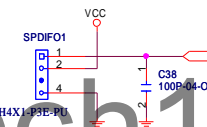
Cd



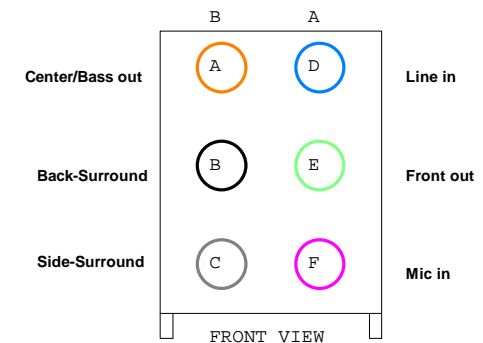
FRONT-AUDIO



SPDIF-OUT



TOP VIEW



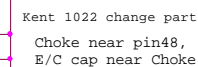
FRONT VIEW

AUDIO ALC892(PANEL)			
Size	Document Number	H55H-M3	
Custom			Rev 1.0
Date:	Wednesday, December 23, 2009	Sheet	25 of 31

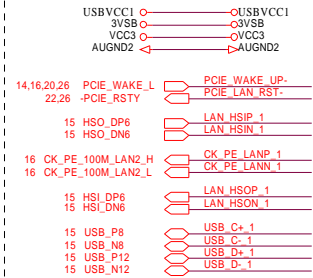
Pin 1-20 connector pinout diagram:

- Pin 1: USBVCC1
- Pin 2: 3VSB
- Pin 3: VCC3
- Pin 4: AUGND2
- Pin 5: PCIE_WAKE_L
- Pin 6: PCIE_RSTY
- Pin 7: HSDQ_DNS
- Pin 8: HSDQ_DNS
- Pin 9: CK_PE_LAMP
- Pin 10: CK_PE_LAMP
- Pin 11: LAN_HSOP
- Pin 12: LAN_HSON
- Pin 13: USB_C+
- Pin 14: USB_C-
- Pin 15: USB_D+
- Pin 16: USB_D-
- Pin 17: USBVCC1
- Pin 18: 3VSB
- Pin 19: VCC3
- Pin 20: AUGND2

	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3VSB供應	3.3V 3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應



External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

新手提醒:

- LAN_HSOP/N請接到SB的PCIE RX端
- LAN_HSIOP/N請接到SB的PCIE TX端
- LAN_HSIOP/N在SB的PCIE TX端要記放AC coupling cap

RTL8103EL-GR
01-278-103350

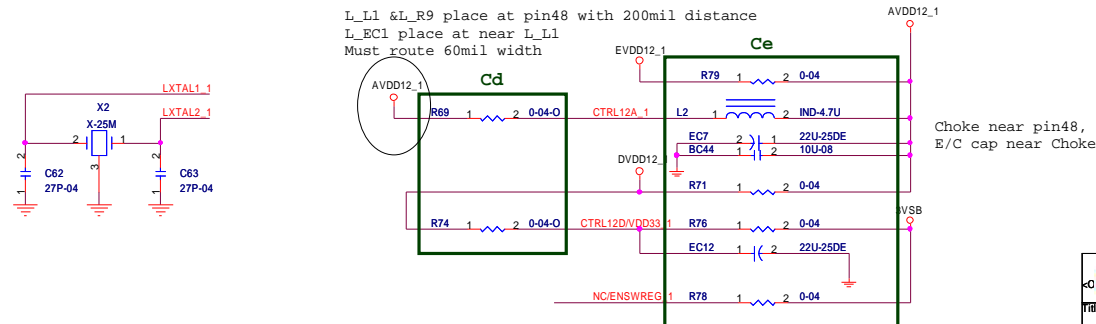
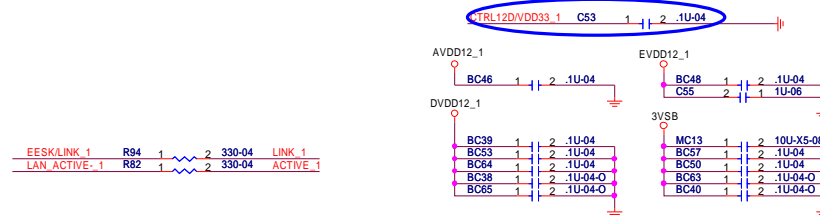
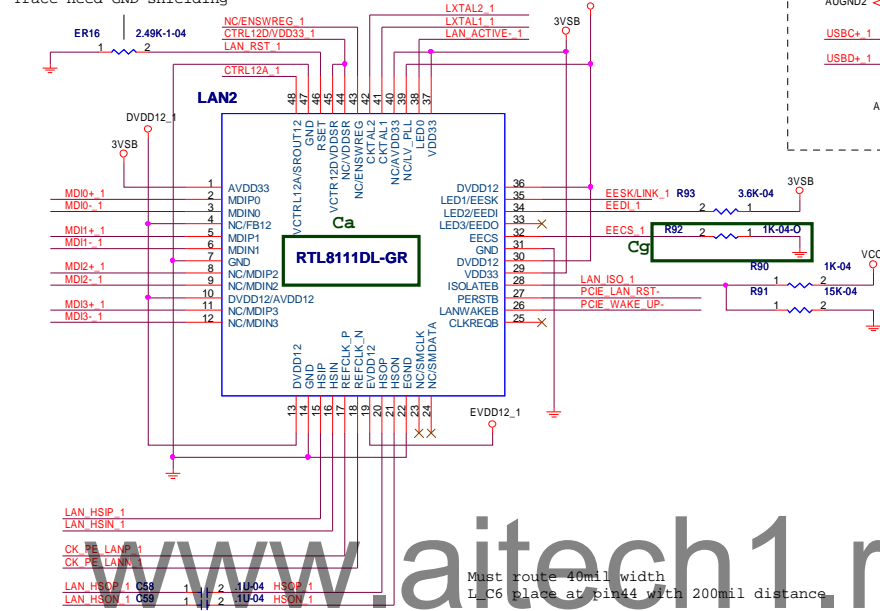
BOM Difference

	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100
Cg	X	V

Power Difference

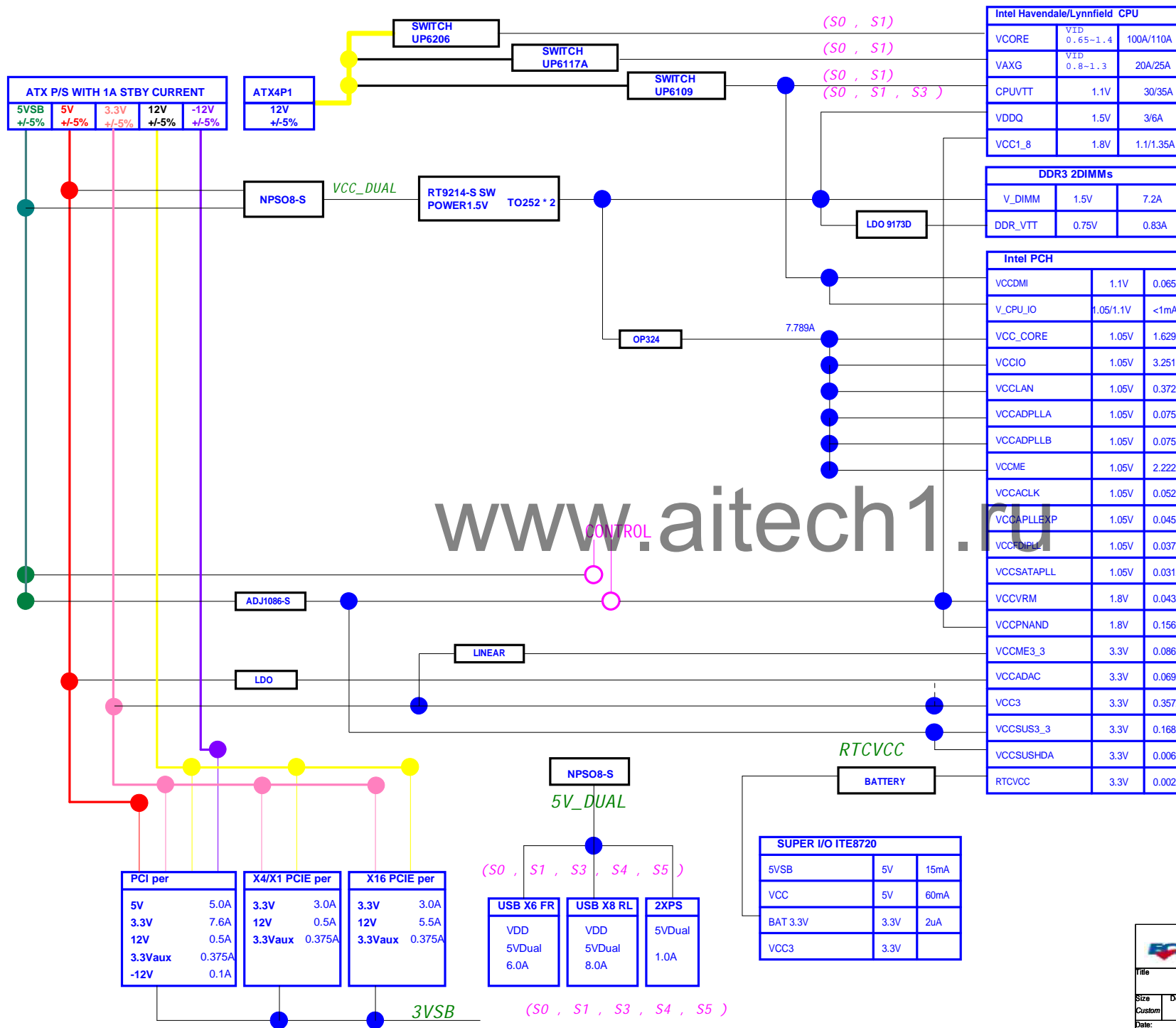
	RTL8111D	RTL8103E
AVDD33	3.3V	3.3V
VDD33	3VSB供應	3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

RSET電阻需close to LAN
Trace need GND shielding



Elitegroup Computer Systems			
PCIE LAN2 RTL8111DL/8103EL			
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FANS		
V12s0	12V	200mA

CLK GEN		
VDD*	3.3V	10mA

DVI		
V3.3s0	3.3V	180mA

USB2.0		
V5Sdual	5V	0.5A*10

SPI		
VCC	5V	10mA

AZALIA		
DVDD	3.3V	0.3A
AVDD	5V	0.1A


LAN		
VDD33	3.3V	58mA
VDD12	5V	289mA

Intel Havendale/Lynfield CPU		
VCORE	VID 0.65~1.4	100A/110A
VAXG	VID 0.8~1.3	20A/25A
CPUVTT	1.1V	30/35A
VDDQ	1.5V	3/6A
VCC1_8	1.8V	1.1/1.35A

DDR3 2DIMMs		
V_DIMM	1.5V	7.2A
DDR_VTT	0.75V	0.83A

Intel PCH		
VCCDMI	1.1V	0.065A
V_CPU_IO	1.05/1.1V	<1mA
VCC_CORE	1.05V	1.629A
VCCIO	1.05V	3.251A
VCCLAN	1.05V	0.372A
VCCADPLLA	1.05V	0.075A
VCCADPLLB	1.05V	0.075A
VCCME	1.05V	2.222A
VCCCLK	1.05V	0.052A
VCCAPLLEXP	1.05V	0.045A
VCCDIPLL	1.05V	0.037A
VCCSATAPLL	1.05V	0.031A
VCCVRM	1.8V	0.043A
VCCPNAND	1.8V	0.156A
VCCME3_3	3.3V	0.086A
VCCADAC	3.3V	0.069A
VCC3	3.3V	0.357A
VCCSUS3_3	3.3V	0.168A
VCCSUSHDA	3.3V	0.006A
RTCVCC	3.3V	0.002A

SUPER I/O ITE8720		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA
VCC3	3.3V	

Elitegroup Computer Systems

Power Delivery Chart

Size Custom

Document Number

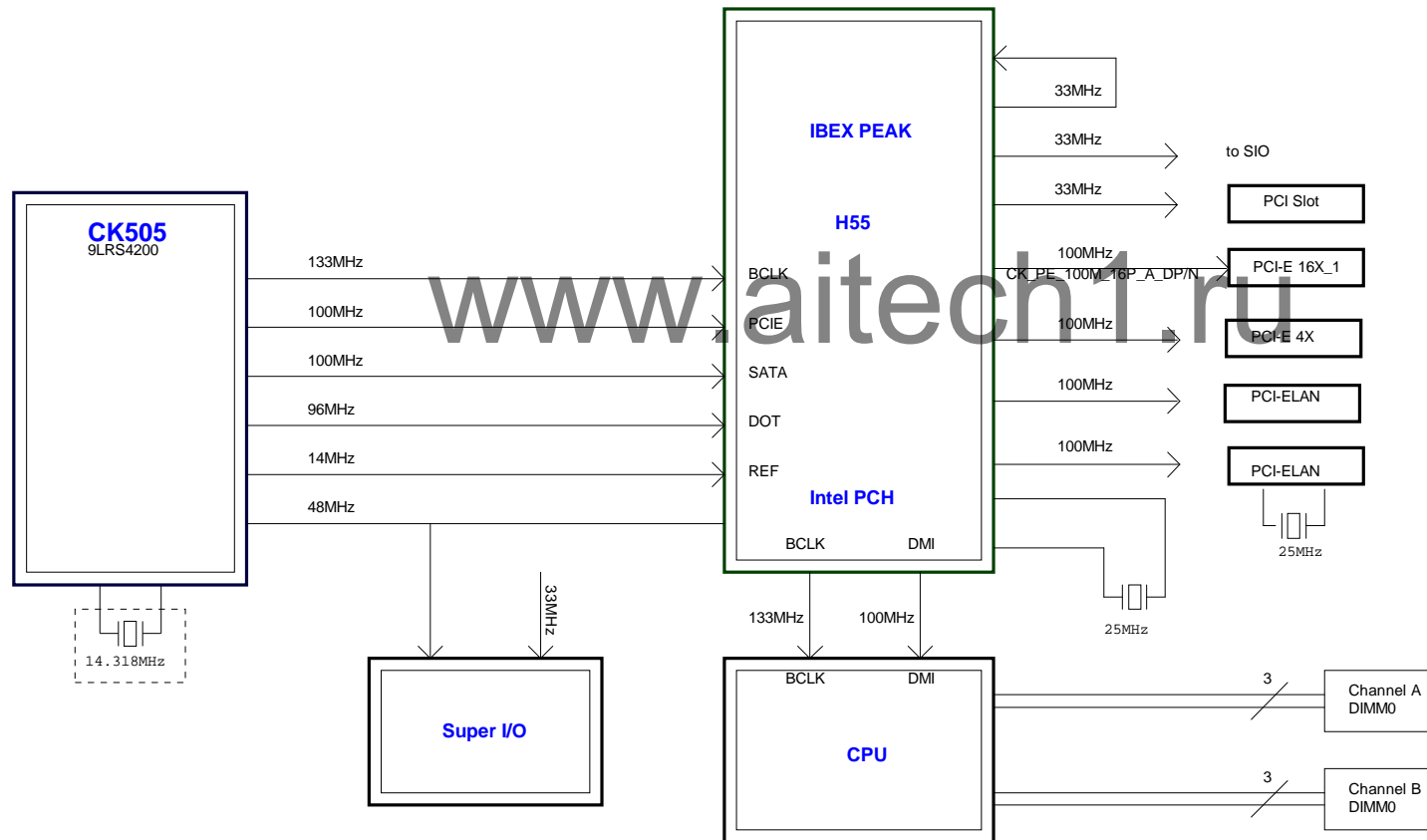
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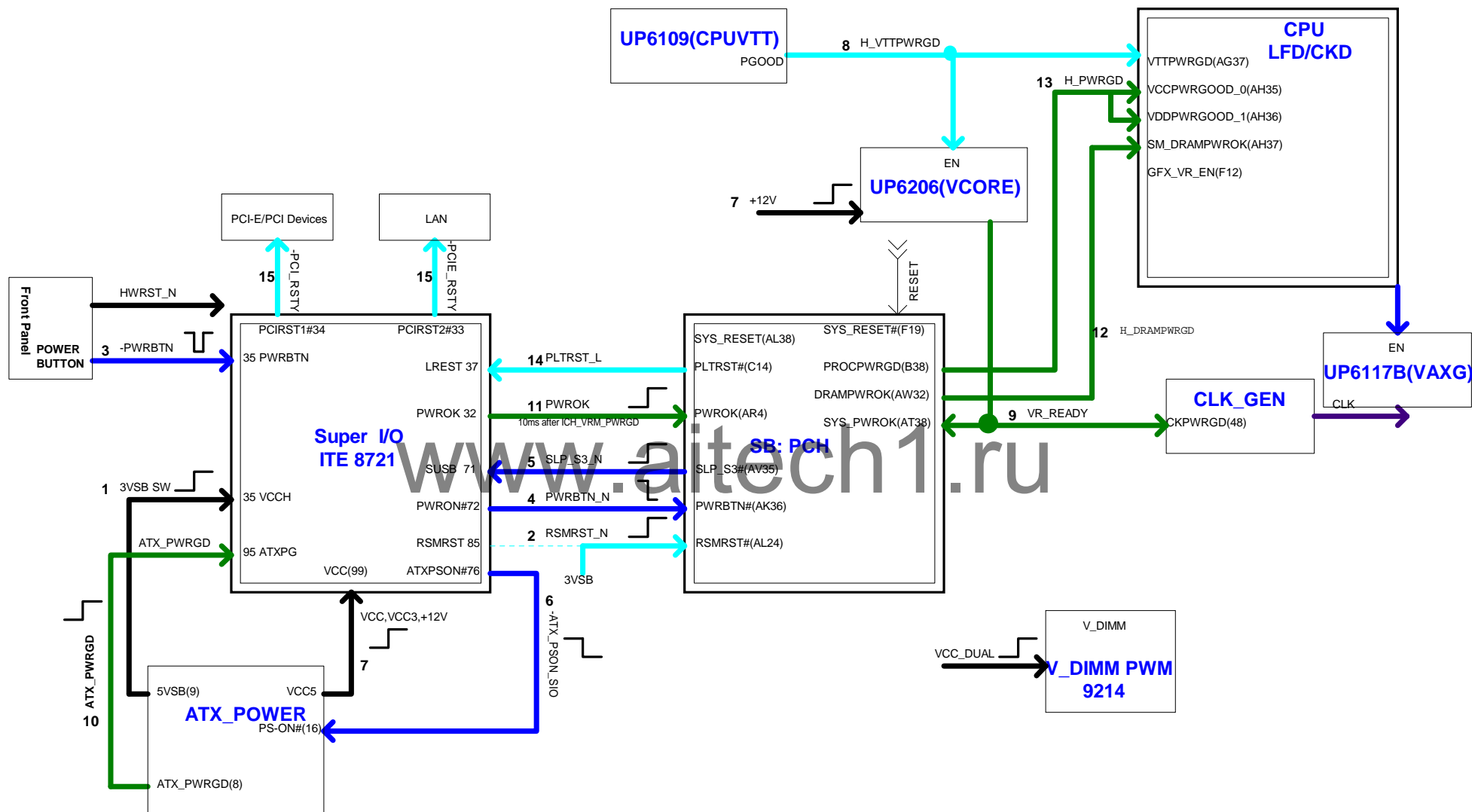
H55H-M3

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Rev 1.0

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PCH STRAPS TABLE																
	H	L	DESCRIPTION	Default												
PGNT-3	(inter pu)	*Top Boot Block(-0)	A16 SWAP OVERRIDE Low: OVERRIDE	TestPoint												
PGNT-1, PGNT-0	<table border="1"><tr><td>BOOT_DEVICE</td><td>GNT0</td><td>GNT1</td></tr><tr><td>LPC</td><td>0</td><td>0</td></tr><tr><td>PCI</td><td>0</td><td>1</td></tr><tr><td>*SPI</td><td>1</td><td>1</td></tr></table>	BOOT_DEVICE	GNT0	GNT1	LPC	0	0	PCI	0	1	*SPI	1	1		Inter Pu Hi	SPI
BOOT_DEVICE	GNT0	GNT1														
LPC	0	0														
PCI	0	1														
*SPI	1	1														
PGNT-2	(inter pu)	*(-0),Desktop not pull low	DMI AC Coupling Low: Full Voltage Mode	TestPoint												
HDA_SDO	*POWERED BY EPW(-0)	POWERED BY CORE(inter pu)	NAND VCCQ PWR WELL SEL													
HDA_SYNC	*1.5V(-0)	1.8V	OD PLL VR SUPPLY SEL													
SPI_MOSI	*EN(-0)	DIS(inter pu)	TPM FUNCTIONALITY TPM DISABLED WHEN SAMPLED LOW													
NVR_ALE	*(10K)		DANBURY Technology Enable Enable When Sampled High													
NVR_CLE	*(-0)		DMI Termination Voltage DC Coup: TX/RX To VCC Is Sampled High													
INIT3_3V_N		*(-0)	Configurable CPU Output, Stronger If Low													
SPKR	*EN(1K)	DIS	STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).													
PCH_INTVRMEN	*EN(390K)		ENABLE INTERGRATED 1.05V SUS VRM.													
PCH_PU_GP33																
IGC_EN_N		*EN	INTEGRATED CLOCK CHIP ENABLE, Stuff Low For Full Clock Integration Enable.													
VCCVRM_EN	*EN(inter pu)	DIS(-0)	OD PLL VR(VccCLK,VccaplleXP, VccFDIPLL,VccSATAPLL; DG P383)													
PCH_GP15	*EN(10K)	DIS	INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) WITH CONFIDENTIALITY													

PCI ROUTING

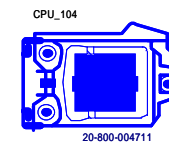
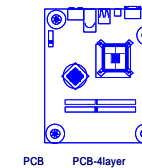
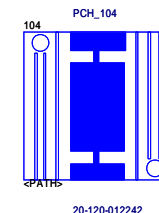
PCI1	AD17	INTA,B,C,D	PREQ-0	PGNT-0
PCI2	AD18	INTB,C,D,A	PREQ-1	PGNT-1

FAN_TAC1	CPU_FAN
FAN_CTL1	CPU_FAN
TMPIN1	SYS_Temp
VIN0	VCORE
VIN1	V_DIMM



1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

做BOM請把(104)加回Reference後面



104,GPIO, IRQ, IDSEL MAP		
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